1. A silicon controlled rectifier formed on a substrate comprising:

a first well region lightly doped with impurities of a first conductivity type formed on said substrate;

a second well region formed within said first well region and lightly doped with impurities of a second conductivity type;

a first diffusion region formed within said second well and heavily doped with the impurities of the first conductivity type;

a second diffusion region formed within said first well region at a second distance from the first diffusion region and heavily doped with impurities of the second conductivity type; and

a heavily doped polycrystalline layer formed at the surface of said substrate and placed between the s and astride a junction of the first well region and the second well region to form a bounding component to prevent silicide formation at junctions of the first diffusion region and the second well region, the first well region and the second region, and the second diffusion region and the first well region during fabrication of said silicon controlled rectifier.

2. The silicon controlled rectifier of claim 1 wherein said heavily doped polycrystalline layer permits a series resistance of said silicon controlled rectifier to be smaller for a more efficient operation.

3. The silicon controlled rectifier of claim 1 wherein the heavily doped polycrystalline layer is connected to bias said heavily doped polycrystalline silicon layer such that salicide shorting is prevented said first and second diffusion regions and preventing of accidental formation of an inversion region under said heavily doped polycrystalline layer.

4. The silicon controlled rectifier of claim 3 wherein said heavily doped polycrystalline silicon layer is connected to the second diffusion region.

5. The silicon controlled rectifier of claim 1 wherein the first diffusion region is linked to a voltage source which provides a relatively large voltage which when said relatively large voltage exceeds said snapback voltage, said silicon controlled rectifier conducts.

6. The silicon controlled rectifier of claim 4 wherein the first well region, the second well region, said highly doped polycrystalline silicon layer, and the second diffusion are power supply connection.

7. The silicon controlled rectifier of claim 6 wherein a first parasitic resistance formed within said first well region and a second parasitic resistance formed within said second well region act to bias a first and second gate of said silicon controlled rectifier to turn-on said silicon controlled rectifier.

8. An ESD protection circuit formed at an input/output of an integrated circuit to protect said integrated circuit from damage caused by an ESD event, said ESD protection circuit comprising:

a polycrystalline silicon bounded SCR connected between a signal input/output interface of said integrated circuit and a power supply connection of said integrated circuit, said polycrystalline silicon bounded SCR comprising:

a first well region lightly doped with impurities of a first conductivity type formed on said substrate and connected to said power supply connection,

a second well region formed within said first well region and lightly doped with impurities of a second conductivity type,

a first diffusion region formed within said second well, heavily doped with the impurities of the first conductivity type, and connected to said signal input/output interface,

a second diffusion region formed within said first well region at a second distance from the first diffusion region, heavily doped with impurities of the second conductivity type, and connected to said power supply connection, and

a first heavily doped polycrystalline layer formed at the surface of said substrate and placed between the first and second diffusion regions and astride a junction of the first well region and the second well region to form a bounding component to prevent silicide formation at junctions of the first diffusion region and the second well region,

the first well region and the second region, and the second diffusion region and the first well region during fabrication of said silicon controlled rectifier; and

a biasing circuit connected to said polycrystalline silicon bounded SCR to bias said polycrystalline silicon bounded SCR to turn on more rapidly during said ESD event.

9. The ESD protection circuit of claim 8 further comprising at least one diode formed on said substrate and connected between said signal input/output interface and an anode connection of said polycrystalline silicon bounded SCR to increase a holding voltage for said polycrystalline silicon bounded SCR when said polycrystalline silicon bounded SCR is turned on.

10. The ESD protection circuit of claim 8 wherein said biasing circuit: comprises:

a polycrystalline silicon bounded diode connected from the signal input/output interface, said polycrystalline silicon bounded diode comprising:

the first diffusion region,

the second well region, and

a second heavily doped polycrystalline layer formed at the surface of said substrate and placed adjacent to the first diffusion region and astride a junction of the second well

region and first diffusion region to form a bounding component to prevent silicide formation at said junction of the first diffusion region and the second well region during fabrication of said polycrystalline silicon bounded diode;

wherein said junction of the first diffusion region and the second well region forms said polycrystalline bounded diode; and

a first resistance formed of material of the second well from a first gate of said polycrystalline silicon bounded SCR to a third diffusion region formed within said second well, heavily doped with the impurities of the second conductivity type, and connected to said power supply connection to provide a low resistance path to said second well from said power supply connection.

11. The ESD protection circuit of claim 10 wherein said biasing circuit: further comprises:

a second resistance formed material of the second well from said first gate to said first diffusion region.

12. The ESD protection circuit of claim 8 wherein said biasing circuit: comprises:

a first resistor connected from the signal input/output interface to the first gate of said polycrystalline silicon bounded SCR; and

a first capacitor connected from the first gate of the polycrystalline silicon bounded SCR to said power supply connection;

wherein upon said ESD event, a top plate of said capacitor connected to said gate of the polycrystalline bounded SCR is a virtual ground and said polycrystalline silicon bounded SCR is activated.

13. The ESD protection circuit of claim 8 wherein said biasing circuit: comprises:

a plurality of serially connected diodes, where a first diode of said plurality of serially connected diodes is connected to the signal input/output interface and a last diode of said plurality of serially connected diodes is connected to a second gate of said polycrystalline silicon bounded SCR; and

a second resistor connected from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection;

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the polycrystalline silicon bounded SCR to turn on.

14. The ESD protection circuit of claim 8 wherein said biasing circuit: comprises:

a resistor/capacitor biasing circuit comprising:

a first resistor connected from the signal input/output interface to the first gate of said polycrystalline silicon bounded SCR, and

a first capacitor connected from the first gate of the polycrystalline silicon bounded SCR to said power supply connection,

wherein upon occurrence of said ESD event, a top plate of said capacitor connected to said gate of the polycrystalline bounded SCR virtually connected to said power supply connection and said polycrystalline silicon bounded SCR is activated;

a diode triggering biasing circuit comprising:

a plurality of serially connected diodes, where a first diode of said plurality of serially connected diodes is connected to the signal input/output interface and a last diode of said plurality of serially connected diodes is connected to a second gate of said polycrystalline silicon bounded SCR, and

a second resistor connected from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection,

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the polycrystalline silicon bounded SCR to turn on.

15. The ESD protection circuit of claim 8 wherein said biasing circuit comprises:

a resistor/capacitor biasing circuit comprising:

a second resistor connected from the signal input/output interface, said second resistor including a first metal oxide semiconductor transistor of a first conductivity type with a source connected to the signal input/output interface and a gate connected so as to have a voltage level approximately equal the power supply connection of said integrated circuit, and

a second capacitor connected between the second resistor and said power supply connection, said second capacitor including a second metal oxide semiconductor transistor with a drain and source connected to a drain of said second metal oxide semiconductor transistor and a gate connected to said power supply connection; and

an SCR triggering circuit with an input connected to a junction of said second resistor and said second capacitor, said SCR trigger circuit comprising:

a plurality of serially connected inverter circuits,

wherein an input to a first inverter of the plurality of serially connected inverter circuits is connected to the junction of said second resistor and said second capacitor,

wherein an in phase output that provides a signal that is in phase with said input to said first inverter is connected to the first gate of said polycrystalline silicon bounded SCR,

wherein an out-of-phase output that provides a signal that is out of phase with said input to said first inverter is connected to the second gate of said polycrystalline silicon bounded SCR;

wherein upon occurrence of said ESD event, a top plate of said second capacitor is virtually connected to said power supply connection to cause said plurality of serially connected inverters to activate with a sharp transition and clearly defined windown to trigger the polycrystalline silicon bounded SCR to turn on.

16. The ESD protection circuit of claim 15 further comprising:

a diode connected between the polycrystalline silicon bounded SCR and said signal input/output interface of said integrated circuit to increase a holding voltage of said polycrystalline silicon bounded SCR.

17. The ESD protection circuit of claim 15 wherein said biasing circuit further comprises:

a diode connected between said first inverter said plurality of serially connected inverters and said signal input/output interface of said integrated circuit to avoid unintended triggering of said ESD protection circuit.

18. The ESD protection circuit of claim 8 wherein said biasing circuit comprises:

a resistor/capacitor biasing circuit comprising:

a third resistor connected from the signal input/output interface, said third resistor including a second metal oxide semiconductor transistor of the first conductivity type with a source connected to the signal input/output interface and a gate connected so as to have a voltage level approximately equal the power supply connection of said integrated circuit, and

a third capacitor connected between the third resistor and said power supply connection, said third capacitor including a fourth metal oxide semiconductor transistor with a drain and source connected to a drain of said third metal oxide semiconductor transistor; and

an SCR triggering circuit with an input connected to a junction of said third resistor and said third capacitor, said SCR trigger circuit comprising:

an inverter including:

an input connected to the junction of said second resistor and said second capacitor,

a weak feedback pull-up metal oxide semiconductor transistor to provide a sharp transition and a clearly defined window when said polycrystalline silicon bounded SCR is turned on,

an in phase output that provides a signal that is in phase with said input to said inverter is connected to the first gate of said polycrystalline silicon bounded SCR, and

an out-of-phase output that provides a signal that is out of phase with said input to said inverter is connected to the second gate of said polycrystalline silicon bounded SCR;

wherein upon occurrence of said ESD event, a top plate of said second capacitor is virtually connected to said power supply connection to cause said inverter to activate with the sharp transition and the clearly defined window to trigger the polycrystalline silicon bounded SCR to turn on.

19. The ESD protection circuit of claim 15 further comprising:

a diode connected between the polycrystalline silicon bounded SCR and said signal input/output interface of said integrated circuit to increase a holding voltage of said polycrystalline silicon bounded SCR.

20. The ESD protection circuit of claim 15 wherein said biasing circuit further comprises:

a diode connected between said inverter and said signal input/output interface of said integrated circuit to avoid unintended triggering of said ESD protection circuit.

21. The ESD protection circuit of claim 8 wherein said heavily doped polycrystalline layer of the polycrystalline silicon bounded SCR permits a series resistance of said polycrystalline silicon bounded SCR to be smaller for a more efficient operation.

22. The ESD protection circuit of claim 8 wherein the heavily doped polycrystalline layer is connected to bias said heavily doped polycrystalline silicon layer such that silicide shorting is prevented said first and second diffusion regions and preventing of accidental formation of an inversion region under said heavily doped polycrystalline layer.

23. The ESD protection circuit of claim 22 wherein saidheavily doped polycrystalline silicon layer is connected to the second diffusion region.

24. The ESD protection circuit of claim 22 wherein the first diffusion region is linked to a voltage source which provides a relatively large voltage during said ESD event which when said relatively large voltage exceeds said snapback voltage, said polycrystalline silicon bounded SCR conducts.

25. The ESD protection circuit of claim 23 wherein the first well region, the second well region, said highly doped polycrystalline silicon layer, and the second diffusion are power supply connection .

26. The ESD protection circuit of claim 25 wherein a first parasitic resistance formed within said first well region and a second parasitic resistance formed within said second well region act to bias a first and second gate of said silicon controlled rectifier to turn-on said polycrystalline silicon bounded SCR.

27. A method for fabricating a silicon controlled rectifier on a substrate comprising the steps of:

forming a first well region lightly doped with impurities of a first conductivity type on a surface of said substrate;

forming a second well region within said first well region by lightly doping said second well region with impurities of a second conductivity type, said impurities of the second conductivity type having a polarity opposite the impurities of the first conductivity type;

forming a first diffusion region within said second well by heavily doping said first diffusion region with the impurities of the first conductivity type;

forming a second diffusion region within said first well region at a second distance from the first diffusion region by heavily doping said second diffusion region with impurities of the second conductivity type; and

forming a heavily doped polycrystalline layer at the surface of said substrate and between the first and second diffusion regions and astride a junction of the first well region and the second well region to form a bounding component to prevent silicide formation at junctions of the first diffusion region and the second well region, the first well region and the second region, and the second diffusion region and the first well region during fabrication of said silicon controlled rectifier.

28. The method of claim 27 wherein said heavily doped polycrystalline layer permits a series resistance of said silicon controlled rectifier to be smaller for a more efficient operation.

29. The method of claim 27 further comprises the step of connecting the heavily doped polycrystalline layer to bias said heavily doped polycrystalline silicon layer such that silicide shorting is prevented said first and second diffusion regions and preventing of accidental formation of an inversion region under said heavily doped polycrystalline layer.

30. The method of claim 29further comprising the step of connecting said heavily doped polycrystalline silicon layer to the second diffusion region.

31. The method of claim 27 further comprising the step of linking the first diffusion region to a voltage source which provides a relatively large voltage which when said relatively large voltage exceeds said snapback voltage, said silicon controlled rectifier conducts.

32. The method of claim 30further comprising the step of linking the first well region, the second well region, said highly doped polycrystalline silicon layer, and the second diffusion to a return of the voltage source.

33. The method of claim 32 wherein a first parasitic resistance formed within said first well region and a second parasitic resistance formed within said second well region act to bias a first and second gate of said silicon controlled rectifier to turn-on said silicon controlled rectifier.

34. A method for forming an ESD protection circuit formed at an input/output interface of an integrated circuit formed on a substrate to protect said integrated circuit from damage caused by an ESD event, said ESD protection circuit comprising:

forming a polycrystalline silicon bounded SCR on a surface of said substrate by the steps of :

forming a first well region lightly doped with impurities of a first conductivity type on a surface of said substrate,

forming a second well region within said first well region by lightly doping said second well region with impurities of a second conductivity type, said impurities of the second conductivity type having a polarity opposite from the impurities of the first conductivity type,

forming a first diffusion region within said second well by heavily doping said first diffusion region with the impurities of the first conductivity type,

forming a second diffusion region within said first well region at a second distance from the first diffusion region by heavily doping said second diffusion region with impurities of the second conductivity type, and

forming a heavily doped polycrystalline layer at the surface of said substrate and between the first and second diffusion regions and astride a junction of the first well region and the second well region to form a bounding component to prevent silicide formation at junctions of the first diffusion region and the second well region, the first well region and the second region, and the second diffusion

region and the first well region during fabrication of said silicon controlled rectifier;

connecting said polycrystalline silicon bounded SCR between a signal input/output interface of said integrated circuit and a power supply connection of said integrated circuit;

forming a biasing circuit; and

connecting said biasing circuit to said polycrystalline silicon bounded SCR to bias said polycrystalline silicon bounded SCR to turn on more rapidly during said ESD event.

35. The method of claim 34 further comprising the steps of:

forming at least one diode on said substrate; and

connecting said diode between said signal input/output interface and an anode connection of said polycrystalline silicon bounded SCR to increase a holding voltage for said polycrystalline silicon bounded SCR when said polycrystalline silicon bounded SCR is turned on.

36. The method of claim 34 wherein forming said biasing circuit: comprises the steps of:

forming a polycrystalline silicon bounded diode said polycrystalline silicon bounded diode by the steps of:

forming the first diffusion region,

forming the second well region, and

forming a second heavily doped polycrystalline layer at the surface of said substrate and placed adjacent to the first diffusion region and astride a junction of the second well region and first diffusion region to form a bounding component to prevent silicide formation at said junction of the first diffusion region and the second well region during fabrication of said polycrystalline silicon bounded diode;

wherein said junction of the first diffusion region and the second well region forms said polycrystalline bounded diode; and

connecting said polycrystalline silicon bounded diode to the signal input/output interface,

forming a third diffusion region within said second well by heavily doping said third diffusion region with the impurities of the second conductivity type,

forming a first resistance of material of the second well from a first gate of said polycrystalline silicon bounded SCR to said third diffusion region, and

connecting said third diffusion region to said power supply connection to provide a low resistance path to said second well from said power supply connection.

37. The method of claim 36wherein forming said biasing circuit further comprises the steps of:

forming a second resistance of the material of the second well from said first gate to said first diffusion region.

38. The method of claim 34 wherein forming said biasing circuit: comprises the steps of:

forming a first resistor from the signal input/output interface to the first gate of said polycrystalline silicon bounded SCR; and

forming a first capacitor from the first gate of the polycrystalline silicon bounded SCR to said power supply connection;

wherein upon said ESD event, a top plate of said capacitor connected to said gate of the polycrystalline bounded SCR virtually connected to said power supply connection and said polycrystalline silicon bounded SCR is activated.

39. The method of claim 34 wherein said biasing circuit: comprises the steps of:

forming a plurality of serially connected diodes;

connecting a first diode of said plurality of serially connected diodes to the signal input/output interface;

connecting a last diode of said plurality of serially connected diodes to a second gate of said polycrystalline silicon bounded SCR; and

forming a second resistor from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection;

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the polycrystalline silicon bounded SCR to turn on.

40. The method of claim 34 wherein forming said biasing circuit: comprises the steps of:

forming a resistor/capacitor biasing circuit by the steps of:

forming a first resistor from the signal input/output interface to the first gate of said polycrystalline silicon bounded SCR, and

forming a first capacitor from the first gate of the polycrystalline silicon bounded SCR to said power supply connection,

wherein upon said ESD event, a top plate of said capacitor connected to said gate of the polycrystalline bounded SCR

virtually connected to said power supply connection and said polycrystalline silicon bounded SCR is activated.

forming a diode triggering biasing circuit by the steps of:

forming a plurality of serially connected diodes;

connecting a first diode of said plurality of serially connected diodes to the signal input/output interface,

connecting a last diode of said plurality of serially connected diodes to a second gate of said polycrystalline silicon bounded SCR, and

forming a second resistor from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection,

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the polycrystalline silicon bounded SCR to turn on.

41. The method of forming the ESD protection circuit of claim 34 wherein forming said biasing circuit comprises the steps of:

creating a resistor/capacitor biasing circuit by the steps of:

forming a third resistor by the steps of:

creating a second metal oxide semiconductor transistor of the first conductivity type,

connecting a source of said second metal oxide semiconductor transistor to the signal input/output interface, and

connecting a gate of said second metal oxide semiconductor transistor so as to have a voltage level approximately equal the power supply connection of said integrated circuit, and

forming a third capacitor by the steps of;

creating a fourth metal oxide semiconductor transistor,

connecting a drain and a source of said fourth metal oxide semiconductor transistor to a drain of said third metal oxide semiconductor transistor and, and

connecting a gate of said fourth metal oxide semiconductor to said power supply connection; and

forming an SCR triggering circuit by the steps of:

forming an inverter,

connecting an input of said inverter to the junction of said second resistor and said second capacitor,

forming a weak feedback pull-up metal oxide semiconductor transistor within said inverter to provide a sharp transition and a clearly defined window when said polycrystalline silicon bounded SCR is turned on,

connecting an in phase output of said inverter to the first gate of said polycrystalline silicon bounded SCR, said in phase output providing a signal that is in phase with said input to said inverter and

connecting an out-of-phase output of said inverter to the second gate of said polycrystalline silicon bounded SCR, said inverter providing a signal that is out of phase with said input to said inverter; and

connecting an input of the SCR triggering circuit to a junction of said third resistor and said third capacitor,

wherein upon occurrence of said ESD event, a top plate of said second capacitor is virtually connected to said power supply connection to cause said inverter to activate with a sharp transition and clearly defined windown to trigger the polycrystalline silicon bounded SCR to turn on.

42. The method of forming the ESD protection circuit of claim 41 further comprising the steps of :

connecting a diode between the polycrystalline silicon bounded SCR and said signal input/output interface of said integrated circuit to increase a holding voltage of said polycrystalline silicon bounded SCR.

43. The method of forming the ESD protection circuit of claim 41 wherein forming said biasing circuit further comprises the step of :

connecting a diode between said inverter and said signal input/output interface of said integrated circuit to avoid unintended triggering of said ESD protection circuit.

44. The method of forming the ESD protection circuit of claim 34 wherein forming said biasing circuit comprises the steps of :

creating a resistor/capacitor biasing circuit by the steps of:

forming a third resistor by the steps of:

creating a second metal oxide semiconductor transistor of the first conductivity type,

connecting a source of said second metal oxide semiconductor transistor to the signal input/output interface, and

connecting a gate of said second metal oxide semiconductor transistor so as to have a voltage level approximately equal the power supply connection of said integrated circuit, and

forming a third capacitor by the steps of;

creating a fourth metal oxide semiconductor transistor,

connecting a drain and a source of said fourth metal oxide semiconductor transistor to a drain of said third metal oxide semiconductor transistor and, and

connecting a gate of said fourth metal oxide semiconductor to said power supply connection; and

forming an SCR triggering circuit said SCR trigger circuit comprising:

an inverter including:

an input connected to the junction of said second resistor and said second capacitor,

a weak feedback pull-up metal oxide semiconductor transistor to provide a sharp transition and a clearly defined window when said polycrystalline silicon bounded SCR is turned on,

an in phase output that provides a signal that is in phase with said input to said inverter is connected to the first gate of said polycrystalline silicon bounded SCR, and

an out-of-phase output that provides a signal that is out of phase with said input to said inverter is connected to the second gate of said polycrystalline silicon bounded SCR; and

connecting an input of said SCR triggering circuit to a junction of said third resistor and said third capacitor;

wherein upon occurrence of said ESD event, a top plate of said second capacitor is virtually connected to said power supply connection to cause said inverter to activate with a sharp transition and a clearly defined window to trigger the polycrystalline silicon bounded SCR to turn on.

45. The method of forming the ESD protection circuit of claim 41 further comprising the step of:

connecting a diode between the polycrystalline silicon bounded SCR and said signal input/output interface of said integrated circuit to increase a holding voltage of said polycrystalline silicon bounded SCR.

46. The method of forming the ESD protection circuit of claim 41 wherein forming said biasing circuit further comprises the step of:

connecting a diode between said inverter and said signal input/output interface of said integrated circuit to avoid unintended triggering of said ESD protection circuit.

47. The method of claim 34 wherein said heavily doped polycrystalline layer of the polycrystalline silicon bounded SCR permits a series resistance of said polycrystalline silicon bounded SCR to be smaller for a more efficient operation.

48. The method of claim 34 further comprising the step of connecting the heavily doped polycrystalline layer to bias said heavily doped polycrystalline silicon layer such that silicide shorting is prevented said first and second diffusion regions and preventing of accidental formation of an inversion region under said heavily doped polycrystalline layer.

49. The method of claim 48 further comprising the step of connecting said heavily doped polycrystalline silicon layer to the second diffusion region.

50. The method of claim 48 further comprising the step of linking the first diffusion region to a voltage source which provides a relatively large voltage during said ESD event which when said relatively large voltage exceeds said snapback voltage, said polycrystalline silicon bounded SCR conducts.

51. The method of claim 49 further comprising the step of linking the first well region, the second well region, said highly doped polycrystalline silicon layer, and the second diffusion to a return of the voltage source.

52. The method of claim 51 further comprising the steps of:

forming a first parasitic resistance formed within said first well region and a second parasitic resistance within said second well region act to bias a first and second gate of said silicon controlled rectifier to turn-on said polycrystalline silicon bounded SCR.

53. An ESD protection circuit formed at an input/output of an integrated circuit to protect said integrated circuit from damage caused by an ESD event, said ESD protection circuit comprising:

a shallow trench isolation bounded SCR connected between a signal input/output interface of said integrated circuit and a power supply connection of said integrated circuit; and

a biasing circuit connected to said shallow trench isolation bounded SCR to bias said shallow trench isolation bounded SCR to turn on more rapidly during said ESD event.

54. The ESD protection circuit of claim 53 further comprising at least one diode formed on said substrate and conn cted between said signal input/output interface and an anode connection of said shallow trench isolation bounded SCR

to increase a holding voltage for said shallow trench isolation bounded SCR when said shallow trench isolation bounded SCR is turned on.

55. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

a shallow trench isolation bounded diode connected from the signal input/output interface; and

a first resistance formed of material of the second well from a first gate of said shallow trench isolation bounded SCR to a third diffusion region formed within said second well, heavily doped with the impurities of the second conductivity type, and connected to said power supply connection to provide a low resistance path to said second well from said power supply connection.

56. The ESD protection circuit of claim 55 wherein said biasing circuit: further comprises:

a second resistance formed material of the second well from said first gate to said first diffusion region.

57. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

a first resistor connected from the signal input/output interface to the first gate of said shallow trench isolation bounded SCR; and

a first capacitor connected from the first gate of the shallow trench isolation bounded SCR to said power supply connection;

wherein upon said ESD event, a top plate of said capacitor connected to said gate of the shallow trench isolation bounded virtually connected to said power supply connection and said shallow trench isolation bounded SCR is activated.

58. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

a plurality of serially connected diodes, where a first diode of said plurality of serially connected diodes is connected to the signal input/output interface and a last diode of said plurality of serially connected diodes is connected to a second gate of said shallow trench isolation bounded SCR; and

a second resistor connected from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection;

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the shallow trench isolation bounded SCR to turn on.

59. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

a resistor/capacitor biasing circuit comprising:

a first resistor connected from the signal input/output interface to the first gate of said shallow trench isolation bounded SCR, and

a first capacitor connected from the first gate of the shallow trench isolation bounded SCR to said power supply connection,

wherein upon said ESD event, a top plate of said capacitor connected to said gate of the shallow trench isolation bounded is virtually connected to said power supply connection and said shallow trench isolation bounded SCR is activated;

a diode triggering biasing circuit comprising:

a plurality of serially connected diodes, where a first diode of said plurality of serially connected diodes is connected to the signal input/output interface and a last diode of said plurality of serially connected diodes is connected to a second gate of said shallow trench isolation bounded SCR, and

a second resistor connected from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection,

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the shallow trench isolation bounded SCR to turn on.

60. A method for forming an ESD protection circuit formed at an input/output interface of an integrated circuit formed on a substrate to protect said integrated circuit from damage caused by an ESD event, said ESD protection circuit comprising:

forming a shallow trench isolation bounded SCR on a surface of said substrate;

connecting said shallow trench isolation bounded SCR between a signal input/output interface of said integrated circuit and a power supply connection of said integrated circuit;

forming a biasing circuit; and

connecting said biasing circuit to said shallow trench isolation bounded SCR to bias said shallow trench isolation bounded SCR to turn on more rapidly during said ESD event.

61. The method of claim 60 further comprising the steps of:

forming at least one diode on said substrate; and

connecting said diode between said signal input/output interface and an anode connection of said shallow trench isolation bounded SCR to increase a holding voltage for said shallow trench isolation bounded SCR when said shallow trench isolation bounded SCR is turned on.

62. The method of claim 60 wherein forming said biasing circuit: comprises the steps of:

forming a shallow trench isolation bounded diode said shallow trench isolation bounded diode; and

connecting said shallow trench isolation bounded diode to the signal input/output interface,

63. The method of claim 62 wherein forming said biasing circuit further comprises the steps of:

forming a second resistance of the material of the second well from said first gate to said first diffusion region.

64. The method of claim 60 wherein forming said biasing circuit: comprises the steps of:

forming a first resistor from the signal input/output interface to the first gate of said shallow trench isolation bounded SCR; and

forming a first capacitor from the first gate of the shallow trench isolation bounded SCR to said power supply connection;

wherein upon said ESD event, a top plate of said capacitor connected to said gate of the shallow trench isolation bounded virtually connected to said power supply connection and said shallow trench isolation bounded SCR is activated.

65. The method of claim 60 wherein said biasing circuit: comprises the steps of:

forming a plurality of serially connected diodes;

connecting a first diode of said plurality of serially connected diodes to the signal input/output interface;

connecting a last diode of said plurality of serially connected diodes to a second gate of said shallow trench isolation bounded SCR; and

forming a second resistor from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection;

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the shallow trench isolation bounded SCR to tum on.

66. The method of claim 60 wherein forming said biasing circuit: comprises the steps of:

forming a resistor/capacitor biasing circuit by the steps of:

forming a first resistor from the signal input/output interface to the first gate of said shallow trench isolation bounded SCR, and

forming a first capacitor from the first gate of the shallow trench isolation bounded SCR to said power supply connection,

wherein upon said ESD event, a top plate of said capacitor connected to said gate of the shallow trench isolation bounded virtually connected to said power supply connection and said shallow trench isolation bounded SCR is activated.

forming a diode triggering biasing circuit by the steps of:

forming a plurality of serially connected diodes;

connecting a first diode of said plurality of serially connected diodes to the signal input/output interface,

connecting a last diode of said plurality of serially connected diodes to a second gate of said shallow trench isolation bounded SCR, and

forming a second resistor from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection,

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the shallow trench isolation bounded SCR to turn on.